`

DEENBANDHU CHHOTU RAM UNIVERSITY OF SCIENCE & TECHNOLOGY, MURTHAL (SONEPAT)

SCHEME OF STUDIES & EXAMINATIONS
MASTER OF TECHNOLOGY IN ELECTRONICS & COMMUNICATION ENGINEERING (VLSI DESIGN)
Credit based Scheme w.e.f. 2014-15

SEMESTER I										
SN	**Course No.**	**Course Title**	**Teaching Schedule**		**Marks of Class Work**	**Examination Marks**		**Total Marks**	**Credit**	**Duration of Exam.**
			L	**P**		**Theory**	**Practical**			
1	MTVLSI 501	SOLID STATE DEVICE MODELING & SIMULATION	4	-	25	75	-	100	4	3
2	MTVLSI 503	VLSI FOR OPTICAL INTERCONNECTS	4	-	25	75	-	100	4	3
3	MTVLSI 505	DIGITAL CMOS IC DESIGN	4	-	25	75	-	100	4	3
4	MTVLSI 507	VERILOG BASED DIGITAL SYSTEM DESIGN	4	-	25	75	-	100	4	3
5	MTVLSI 509	ADVANCED COMPUTER ARCHITECTURE	4	-	25	75	-	100	4	3
6	MTVLSI 551	VERILOG BASED DIGITAL SYSTEM DESIGN LAB	-	3	20	-	30	50	1.5	3
7	MTVLSI 553	DIGITAL CMOS IC DESIGN LAB	-	3	20	-	30	50	1.5	3
Total			**20**	**06**	**165**	**375**	**60**	**600**	**23**	**-**

Note:

Students will be allowed to use Non-Programmable Scientific Calculator. However, sharing of calculator will not be permitted in the examination.

`

DEENBANDHU CHHOTU RAM UNIVERSITY OF SCIENCE & TECHNOLOGY, MURTHAL (SONEPAT)

SCHEME OF STUDIES & EXAMINATIONS
MASTER OF TECHNOLOGY IN ELECTRONICS & COMMUNICATION ENGINEERING (VLSI DESIGN)
Credit based Scheme w.e.f. 2014-15

SEMESTER II										
S. No.	**Course No.**	**Course Title**	**Teaching Schedule**		**Marks of Class Work**	**Examination Marks**		**Total Marks**	**Credit**	**Duration of Exam.**
			L	**P**		**Theory**	**Practical**			
1	MTVLSI 502	ANALOG CMOS IC DESIGN	4	-	25	75	-	100	4	3
2	MTVLSI 504	ESD USING AVR MICROCONTROLLER	4	-	25	75	-	100	4	3
3	MTVLSI 506	OPTIMIZATION FOR VLSI DESIGN	4	-	25	75	-	100	4	3
4	MTVLSI 508	LOW POWER VLSI DESIGN	4	-	25	75	-	100	4	3
5		**ELECTIVE I**	4	-	25	75	-	100	4	3
6	MTVLSI 550	ESD USING AVR MICROCONTROLLER LAB	-	3	20	-	30	50	1.5	3
7	MTVLSI 552	ANALOG CMOS IC DESIGN LAB	-	3	20	-	30	50	1.5	3
Total			**20**	**6**	**165**	**375**	**60**	**600**	**23**	**-**

LIST OF ELECTIVES					
ELECTIVE – I		**ELECTIVE – II**		**ELECTIVE – III**	
MTVLSI 560	IC FABRICATION TECHNOLOGY	MTVLSI 661	CMOS RF IC DESIGN	MTVLSI 663	DESIGN OF SEMICONDUCTORS MEMORY
MTVLSI 570	DSP FOR VLSI DESIGN	MTVLSI 671	VLSI SIGNAL PROCESSING	MTVLSI 673	HIGH SPEED VLSI INTERCONNECTS
MTVLSI 580	INTRODUCTION TO MEMS	MTVLSI 681	SYSTEM ON CHIP	MTVLSI 683	HARDWARE SOFTWARE CO-DESIGN
MTVLSI 590	COMPUTATIONAL INTELLIGENT TECHNIQUES FOR VLSI DESIGN	MTVLSI 691	CAD FOR VLSI	MTVLSI 693	ALGORITHM FOR VLSI DESIGN

Note:

1. Student can opt for electives (I, II & III), but they can choose only from a particular row (e.g., if a student opts for MTVLSI 580, he/she has to mandatorily opt for MTVLSI 681 & MTVLSI 683).
2. The choice of students for any elective shall not be binding on the department to offer, if the department does not have expertise. The minimum strength of the students opting for the particular subject shall not be less than 8.
3. The students will be allowed to use non-Programmable Scientific Calculator. However, sharing/exchange of calculator is prohibited in the examination.

`

DEENBANDHU CHHOTU RAM UNIVERSITY OF SCIENCE & TECHNOLOGY, MURTHAL (SONEPAT)

SCHEME OF STUDIES & EXAMINATIONS
MASTER OF TECHNOLOGY IN ELECTRONICS & COMMUNICATION ENGINEERING (VLSI DESIGN)
Credit based Scheme w.e.f. 2015-16

SEMESTER III										
S. No.	**Course No.**	**Course Title**	**Teaching Schedule**		**Marks of Class Work**	**Examination Marks**		**Total Marks**	**Credit**	**Duration of Exam.**
			L	**P**		**Theory**	**Practical**			
1	MTVLSI 601	MIXED SIGNAL IC DESIGN	4	-	25	75	-	100	4	3
2		**ELECTIVE II**	4	-	25	75	-	100	4	3
3		**ELECTIVE III**	4	-	25	75	-	100	4	3
4	MTVLSI 651	DISSERTATION (1ST PHASE)	-	6	100	-	-	100	6	3
5	MTVLSI 653	SEMINAR	-	2	50	-	-	50	2	-
6	MTVLSI 655	PROJECT	-	3	50	-	-	50	1.5	3
7	MTVLSI 657	MIXED SIGNAL IC DESIGN LAB	-	3	20		30	50	1.5	3
Total			**12**	**14**	**265**	**225**	**60**	**550**	**23**	**-**

LIST OF ELECTIVES					
ELECTIVE – I		**ELECTIVE – II**		**ELECTIVE – III**	
MTVLSI 560	IC FABRICATION TECHNOLOGY	MTVLSI 661	CMOS RF IC DESIGN	MTVLSI 663	DESIGN OF SEMICONDUCTORS MEMORY
MTVLSI 570	DSP FOR VLSI DESIGN	MTVLSI 671	VLSI SIGNAL PROCESSING	MTVLSI 673	HIGH SPEED VLSI INTERCONNECTS
MTVLSI 580	INTRODUCTION TO MEMS	MTVLSI 681	SYSTEM ON CHIP	MTVLSI 683	HARDWARE SOFTWARE CO-DESIGN
MTVLSI 590	COMPUTATIONAL INTELLIGENT TECHNIQUES FOR VLSI DESIGN	MTVLSI 691	CAD FOR VLSI	MTVLSI 693	ALGORITHMS FOR VLSI DESIGN

Note:

1. Student can opt for electives (I, II & III), but they can choose only from a particular row only (e.g., if a student opts for MTVLSI 580, he/she has to mandatorily opt for MTVLSI 681 & MTVLSI 683).
2. The choice of students for any elective shall not be binding on the department to offer, if the department does not have expertise. The minimum strength of the students opting for the particular subject shall not be less than 8.
3. The students will be allowed to use non-Programmable Scientific Calculator. However, sharing/exchange of calculator is prohibited in the examination.

`

DEENBANDHU CHHOTU RAM UNIVERSITY OF SCIENCE & TECHNOLOGY, MURTHAL (SONEPAT)

SCHEME OF STUDIES & EXAMINATIONS
MASTER OF TECHNOLOGY IN ELECTRONICS & COMMUNICATION ENGINEERING (VLSI DESIGN)
Credit based Scheme w.e.f. 2015-16

SEMESTER IV										
S. No.	**Course No.**	**Course Title**	**Teaching Schedule**		**Marks of Class Work**	**Examination Marks**		**Total Marks**	**Credit**	**Duration of Exam.**
			L	**P**		**Theory**	**Practical**			
1	MTVLSI 652	DISSERTATION	-	20	50	-	100	150	20	-
Total			**-**	**20**	**50**	**-**	**100**	**150**	**20**	**-**

Note:

Dissertation coordinator will be assigned the load of 1 hour per week excluding his/her own guiding load. However, the dissertation guiding teacher will be assigned a load of one hour per candidate per week.

`

MTVLSI 501 SOLID STATE DEVICE MODELING AND SIMULAION

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

MOSFET Device Physics: Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Carrier Generation and Recombination, Avalanche Process, MOSFET capacitor, Basic operation, Basic modelling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II

Noise Modeling: Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

UNIT III

BSIM4 MOSFET Modeling: Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitic model.

UNIT IV

Other MOSFET Models: The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model.
Modeling of Process Variation and Quality Assurance: Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests

Text Books:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, "Device Modeling for Analog and RF".
2. Ben G. Streetman, "Solid State Electronic Devices", Prentice Hall.

Reference Books:

1. Donald A. Neaman, " Semiconductor physics and devices" Third Edition, McGraw –Hill Pvt Ltd 2007
2. Richard S. Muller, Theodore I. Kamins, "Device Electronics for integrated circuits", Wiley, 3rd Edition 2002.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 503 VLSI FOR OPTICAL INTERCONNECTS

L T P	Credits		Class Work	:	25 Marks
4 - -	4		Theory	:	75 Marks
			Total	:	100 Marks
			Duration of Exam.	:	3 Hrs.

UNIT I

Basic Concepts: Introduction to Optical Communication, Properties of Random Binary data and its generation, Data formats, Effect of Bandwidth limitation on Random data

Optical Devices: Laser diodes: Operation of lasers, types of lasers, optical fibers loss and dispersion, photodiodes: Responsivity and efficiency, PIN diodes, Avalanche diode

UNIT II

Trans-impedance Amplifiers: General considerations: TIA performance parameters, SNR calculation and noise bandwidth, open loop TIA, feedback TIA

Limiting amplifier/ output buffer: General considerations: Performance parameters, cascaded gain stages, AM/PM conversion, broadband technique: inductive peaking, output buffers

UNIT III

Oscillator: General considerations, ring oscillator, LC oscillators, voltage controlled oscillator

Multiplexer and Laser driver: Multiplexers (2:1 mux, mux architecture, Laser and Modulator drivers: performance parameters

UNIT IV

Optical vs Electrical Interconnects: Electrical Interconnects, Optical interconnects, comparison, optical interconnects in system

Text Books:

1. Behzad Razavi, "Design of Integrated circuits for optical communication", McGraw-Hill, 1st Edition, 2002.
2. Hartmut Grabinski, "Interconnects in VLSI Design", Springer, 2012.

Reference Books:

1. Ibrahim Gokce Yayla, "Speed and energy comparison between electrical and electro-optical interconnects and application to optoelectronic computing", University of California, San Diego, 1996.
2. Pascal Berthome, "Optical Interconnections and Parallel Processing: Trends at the Interface", Springer, 2010.
3. Sadik Esener and Philippe Marchand, "Present and Future Needs of Free-Space Optical Interconnects", Springer.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 505 **DIGITAL CMOS IC DESIGN**

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Basic principle of MOS transistor, Introduction to large signal and small signal MOS models for digital design, MOS Switches, Threshold Voltage, Transconductance and output Conductance, Pull-up to Pull-down ratio Calculation

The MOS Inverter: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, BiCMOS Inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Latch-up, Propagation Delay and Power Consumption.

UNIT II

Symbolic and Physical Layout Systems: MOS Layers Stick/Layout Diagrams, Layout Design Rules, Transistor layout, Inverter layout, CMOS digital circuit layout Issues of Scaling, Scaling factor for device parameters.

Performance Estimation: Resistance Estimation, Capacitance Estimation, Inductance Estimation, Switching characteristics, CMOS-gate transistor Sizing.

UNIT III

Combinational & Sequential Logic Structures: CMOS Logic Families - static, dynamic and differential logic families, CMOS Complimentary logic, Pseudo NMOS logic, Dynamic Logic Circuits: Basic principle, non ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking, pass Transistor logic, transmission gates logic circuits, complimentary switch logic, SR latches, Flip flops: JK, D, Master- Slave & Edge triggered. Registers, CMOS Schmitt trigger.

UNIT IV

Subsystem Design: Design of an ALU Subsystem: design 4-bit simple and carry look ahead adder, multiplier design: serial-parallel multiplier, Braun Array, Wallace tree Multiplier, Design of 4-bit Shifter.

CMOS Memory Design: Semiconductor memories, memory chip organization, RAM Cells, dynamic memory cell, Programmable logic arrays

Text Books:

1. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, “Digital Integrated Circuits” Second Edition, PH/Pearson, 2003.
2. D. A. Pucknell and K. Eshraghian, “Basic VLSI Design”, Third Edition, PHI, 1994.

Reference Books:

1. S. M. Kang and Y. Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Third Edition, MH, 2002.
2. W. Wolf, Modern VLSI Design: System on Chip, Third Edition, PH/Pearson, 2002.
3. N. Weste, K. Eshraghian and M. J. S. Smith, Principles of CMOS VLSI Design” Pearson, 2001.
4. John P. Uyemura, CMOS Logic Circuit Design

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 507 VERILOG BASED DIGITAL SYSTEM DESIGN

L T P	Credits			
4 - -	4	Class Work	:	25 Marks
		Theory	:	75 Marks
		Total	:	100 Marks
		Duration of Exam.	:	3 Hrs.

UNIT I

Basic Digital Systems: Introduction to Digital Design, number systems, Boolean Algebra, Combinational Circuits, Sequential Circuits, Timing issues, Electrical Characteristics, Power Dissipation.
Current state of the field: SoC, IP Design, SoPC, Design methodology, System Modelling, Hardware-Software Co-design, Device Technology, Application Domains.

UNIT II

Digital system Design: Top down Approach, Case study, Data Path, Control Path, Controller behaviour and Design, Case study Mealy & Moore Machines, Timing of sequential circuits, Pipelining, Resource sharing, FSM issues (Starring state, Power on Reset, State diagram optimization, Stat, Assignment, Asynchronous Inputs, Output Races, fault Tolerance.
Combinational & Sequencing Circuit Design: Circuit Families, Static CMOS, Ratioed Circuits. Cascade Voltage Switch Logic, Dynamic Circuits. Pass Transistor Circuits, Differential Circuits, Sequencing Static Circuits, Circuit Design of Latches And Flip-Flops. Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers.

UNIT III

Modelling and Synthesis with the Verilog HDL:
Hardware modeling with the Verilog HDL, Encapsulation, modeling primitives, different types of description, Logic system, data types and operators for modeling in Verilog HDL, Verilog Models of propagation delay and net delay path delays and simulation, Inertial delay effects and pulse rejection, Behavioural descriptions in Verilog HDL.
HDL-based Synthesis: Synthesis of combinational logic, Technology-independent design, Styles for synthesis of combinational and sequential logic, Synthesis of finite state machines, Synthesis of gated clocks, Design partitions and hierarchical structures, Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives, Switch-level models in Verilog, Design examples in Verilog.

UNIT IV

Data-path & Array Subsystems: Addition / Subtraction, Comparators, Counters, Coding, multiplication & division, SRAM, DRAM, ROM, Serial access memory, Context-addressable memory.
PLD's & FPGA's: Introduction, Logic Block Architecture, Routing Architecture, Programmable Interconnections, Design Flow, Boundary Scan, Programmable logic devices (PLDs), Programmable gate arrays. Xilinx series FPGAs, Altera complex PLDs, Altera Flex 10K series CPLDs, FPGA-based system design, FPGA fabrics, Combinational network delay, Power and energy optimization sequential machine design styles, Rules for clocking, Performance analysis, Applications.

Text Books:

1. J. F. Wakerly, Digital Design: Principles and Practices, Prentice Hall.
2. N.H.E. Weste, CMOS VLSI Design (3/e), Pearson, 2005

Reference Books:

1. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
2. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.
3. M.D. Ciletti, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.
4. W.Wolf, FPGA- based System Design, Pearson, 2004
5. PLD, FPGA data sheets.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 509 ADVANCED COMPUTER ARCHITECTURE

L	T	P	Credits			
4	-	-	4	Class Work	:	25 Marks
				Theory	:	75 Marks
				Total	:	100 Marks
				Duration of Exam.	:	3 Hrs.

UNIT I

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software Parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.

UNIT II

System Interconnect Architectures:

Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors.

UNIT III

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines.

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

UNIT IV

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design trade-offs, synchronization.

Scalable point – point interfaces: Alpha364 and HT protocols, high performance signalling layer.

Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine check, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system

Text Books:

1. Kai Hwang, "Advanced computer architecture", TMH. 2000
2. D. A. Patterson and J. L. Hennessey, "Computer organization and design", Morgan Kaufmann, 2nd Ed. 2002.

Reference Books:

1. J. P. Hayes, "computer Architecture and organization"; MGH. 1998.
2. Harvey G. Cragon, "Memory System and Pipelined processors" Narosa Publication. 1998.
3. V. Rajaranam& C. S. R. Murthy, "Parallel computer"; PHI. 2002
4. R.K.Ghose, Rajan Moona&Phalguni Gupta, "Foundation of Parallel Processing", Narosa Publications, 2003.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 551 VERILOG BASED DIGITAL SYSTEM DESIGN LAB

L	T	P	Credits		Class Work	:	20 Marks
-	-	3	1.5		Theory	:	30 Marks
					Total	:	50 Marks
					Duration of Exam.	:	3 Hrs.

LIST OF EXPERIMENTS:

1. Write a Verilog code to realize all the logic gates.
2. Write a Verilog code to implement Half Adders, Full adders and Subtracters using Gates.
3. Write a Verilog code to describe the function of Multiplexer and Demultiplexer using different modelling styles.
4. Write a Verilog code to realize D Flip-Flop and D Latch.
5. Write a Verilog code to implement 2:1 Mux and D Latch using Switches.
6. Write a Verilog code to implement Encoders and Decoders Using if-else Statement and case Statement.
7. Write a Verilog code to implement SR Flip Flop using UDP (User Defined Program).
8. Write the Verilog code for a JK Flip-flop, and its test bench. Use all possible combinations of inputs to test its working.
9. Write the hardware description of a 8-bit register with parallel load, shift left and shift right modes of operation and test its operation.
10. Write a Verilog code to realize Up/Down Counter and Divide by 4.5 Counter.
11. Write a Verilog code to describe the function of Synchronous FIFO.
12. Write a Verilog code using FSM to realize a sequence detector (101101).

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTVLSI 507 contents.

`

MTVLSI 553 DIGITAL CMOS IC DESIGN LAB

L	T	P	Credits		Class Work	:	20 Marks
-	-	3	1.5		Theory	:	30 Marks
					Total	:	50 Marks
					Duration of Exam.	:	3 Hrs

LIST OF EXPERIMENTS:

1. Design a CMOS inverter in schematic and simulate for Transient Characteristics.
2. Design a CMOS two input NAND gate, Two input NOR gate, Two input AND gate and Two input OR gate in schematic and simulate for Transient Characteristics.
3. Design the layout of a CMOS Inverter and simulate for DC (Transfer) and Transient characteristics.
4. Design the layout for two inputs NAND gate, two input OR gate, two input AND gate and two input NOR gate and simulate for DC (Transfer) and Transient characteristics.
5. Realized a two input EXOR gate in schematic, draw its layout and simulate for DC (Transfer) and Transient characteristics.
6. To realize a 1 bit full adder in CMOS schematic, design its layout using tool option and simulate for Transient Characteristics.
7. To realize a Boolean expression Y=Not ((A+B)(C+D)E) in schematic, draw its layout and simulate for Transient Characteristics..
8. To realize a 4 X 1 MUX using transmission gates in schematic and simulate for Transient Characteristics..
9. To Realize JK FLIPFLOP in CMOS schematic, design its layout and simulate for Transient Characteristics.
10. To Realize D FLIPFLOP and T FLIPFLOP in CMOS schematic, design its layout and simulate for Transient Characteristics.
11. To realize a four bit asynchronous counter using T flip-flop as a cell in schematic and simulate for Transient Characteristics.
12. To realize a four bit shift register using D flip-flop as a cell in schematic and simulate for Transient Characteristics.

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTVLSI 505 contents.

`

MTVLSI 502 ANALOG CMOS IC DESIGN

L T P	Credits	Class Work	:	25 Marks
4 - -	4	Theory	:	75 Marks
		Total	:	100 Marks
		Duration of Exam.	:	3 Hrs.

UNIT I

CMOS Models: MOS IV Characteristics, Second order effects, Short-Channel Effects, MOS Device Models, Review of Small Signal MOS Transistor Models, Analog CMOS Process (Double Poly Process), MOSFET Noise.
CMOS Sub circuits: MOS Switch, MOS Diode, MOS Active Resistors, Current Sources, CMOS Regulated Cascade current source, Cascade current sink .

UNIT II

Current Mirrors: Simple current mirror, Cascode current Mirror, Widlar current mirror, Wilson Current Mirror
CMOS Amplifier: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.Single transistor Amplifiers stages: Common Drain, Common Gate & Common Source Amplifiers – resistive load, diode connected load, current source load, triode load, source degeneration, Simple Inverting Amplifier, Gilbert Cell, Cascade Amplifier, source follower, cascode amplifiers.

UNIT III

Operational Amplifier: Differential Amplifiers, , Output Amplifiers, Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascades
Advancement in Op-Amp: MOS telescopic-cascode operational amplifiers, MOS Folded-cascade operational amplifiers, gain boosting, Comparison of various topologies, noise in op-amps, op-amp stability and frequency compensation.

UNIT IV

Comparators Comparators Models and Performance, Development of a CMOS Comparator, Design of a Two-Stage CMOS Comparator, Other Types of Comparators.
Oscillator & Switched Capacitor circuits:
Voltage controlled oscillator, Sampling Switches, Switched Capacitor Amplifier, Switched Capacitor integrator and Switched Capacitor filters.

Text Books:
1. Paul B Gray and Robert G Meyer, "Analysis and Design of Analog Integrated Circuits".
2. Allen and Holberg – "CMOS Analog Circuit Design"

Reference Books:
1. D. A. Johns and Martin, "Analog Integrated Circuit Design", John Wiley, 1997.
2. Gregorian and G C Temes, "Analog MOS Integrated Circuits for Signal Processing", John Wiley, 1986.
3. R L Geiger, P E Allen and N R Strader, VLSI Design Techniques for Analog & Digital Circuits, McGraw Hill, 1990.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 504 ESD USING AVR MICROCONTROLLER

L	T	P	Credits			
4	-	-	4	Class Work	:	25 Marks
				Theory	:	75 Marks
				Total	:	100 Marks
				Duration of Exam.	:	3 Hrs.

UNIT I

INTRODUCTION OF EMBEDDED SYSTEMS: Definition, ingredients of embedded system, requirements & challenges of embedded system design, different types of microcontrollers: Embedded microcontrollers, external memory microcontrollers etc., processor architectures: Harvard V/S Princeton, CISC V/S RISC, Microcontroller's memory types, microcontrollers features: clocking, i/o pins, interrupts, timers, and peripherals.

UNIT II

SOFTWARE FOR EMBEDDED SYSTEM DESIGN: Development tools/environments, Assembly language programming style, Interpreters, High level languages, Intel hex format object files, Debugging.

UNIT III

AVR MICROCONTROLLER: Introduction to AVR microcontroller, features of AVR family microcontrollers, different types of AVR microcontroller, architecture, memory access and instruction execution, pipelining, program memory considerations, addressing modes, CPU registers, Instruction set, and simple operations.
FEATURES OF AVR MICROCONTROLLER: Timer: Control Word, mode of timers, simple programming, generation of square wave, Interrupts: Introduction, Control word Simple Programming, generation of waveforms using interrupt, Serial interface using interrupt, Watch-dog timer, Power-down modes of AVR microcontroller, UART, SRAM.

UNIT IV

APPLICATION BASED AVR MICROCONTROLLER: Interfacing of AVR microcontroller with other devices using serial / parallel communication, I2C Protocol, SPI Protocol, ADC/DAC, DC motor controller using PWM,

Text Books:

1. Dananjay V. Gadre, Programming and Customizing the AVR microcontroller‟, McGraw Hill 2001.

Reference Books:

1. John.B..Peatman, "Design with PIC Micro controller", Pearson Education, 1988.
2. Embedded C Programming and the Atmel AVR; Richard H Barnett, Sarah Cox, Larry O'Cull; 2006
3. C Programming for Microcontrollers Featuring ATMEL's AVR Butterfly and WinAVR Compiler; Joe Pardue; 2005.
4. Atmel AVR Microcontroller Primer: Programming & Interfacing; Steven F Barrett, Daniel Pack, Mitchell Thornton; 2007.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 506 OPTIMIZATION FOR VLSI DESIGN

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Operation Research Models, OR Model, Queuing & Simulation Models, Two Variable LP Model, Graphical LP solution, Computer Solution with solver & AMPL, Linear Programming Applications.

Sensitivity & Post Optimal Analysis: LP Model in Equation Form, Algebraic Solution, Simplex Method, Artificial Starting Solution, Sensitivity Analysis, Dual Problem, Primal-Dual Relationships, Economic Interpretation of Duality, Additional Simplex Algorithms, Post Optimal Analysis.

UNIT II

Models: Transportation Models and its variants, Transportation Algorithms, Assignment Models, Shortest Route Problem and its Algorithms, Maximal Flow Model, CPM & PERT**.**

Simulation Modeling: Monte Carlo Simulation, Type of Simulations, Unconstrained Problems, Constrained Problems**,** Direct Search Method, Gradient Method, Separable, Quadratic

UNIT III

Markov Chains: Continuous Review Models, Single & Multi Period Models, Absolute & n-step Transition Probabilities, State in Markov Chain, First Passage Time, Analysis of Absorbing States.

Queuing Models: Elements of Queuing Model, Role of Exponential Distribution, Pure Birth & Death Model.

UNIT IV

Programming: Simplex Method Fundamentals, Bounded Variables Algorithms, Parametric Linear Programming, Goal Programming Algorithms, Integer Linear Programming & Algorithms, Heuristic Programming, Greedy Heuristics, Meta Heuristics, TSP Algorithms (B&B, Cutting Plain, Nearest Neighbour, Reversal Heuristic, Tabu, Simulated Annealing, Genetic).

Text Books:

1. Operation Research By Taha – Pearson
2. Probability & Statistics with Reliability, Queuing & Computer Serine Application- Kishor S. Trivedi – Willey

Reference Books:

1. Mathematical Modeling Principles & Applications-CENGAGE Learning, Frank R. Giordano, William P. Fox.
2. Operation Research, K. Rajagopal – PHI
3. Operation Research Algorithms and Applications by Rathindra P.Sen, PHI

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 508 **LOW POWER VLSI DESIGN**

L	T	P	Credits			
4	-	-	4	Class Work	:	25 Marks
				Theory	:	75 Marks
				Total	:	100 Marks
				Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.
Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation, Power estimation Techniques.

UNIT II

Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation, Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT III

Low Power Techniques: Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT IV

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.
Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

Text Books:
1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997

Reference Books:
1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 550 ESD USING AVR MICROCONTROLLER LAB

L	T	P	Credits		Class Work	:	20 Marks
-	-	3	1.5		Theory	:	30 Marks
					Total	:	50 Marks
					Duration of Exam.	:	3 Hrs.

LIST OF EXPERIMENTS:

1. To study the architecture of AVR Microcontroller & AVR development board.
2. Write an ALP to enter a word from keyboard and to display.
3. Write an ALP to generate 10 KHz & 100KHz frequency using AVR Microcontroller.
4. Write an ALP to interface intelligent LCD display.
5. Write an ALP to interface intelligent LED display.
6. Write an ALP to Switch ON alarm when AVR Microcontroller receive interrupt.
7. Write an ALP to interface AVR microcontroller with other using serial / parallel communication.
8. Write an ALP to I2C Protocol interface.
9. Write an ALP to interface ADC/DAC.
10. Write an ALP to interface DC motor controller using PWM.

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTVLSI 504 contents.

`

MTVLSI 552 ANALOG CMOS IC DESIGN LAB

L	T	P	Credits			
-	-	3	1.5	Class Work	:	20 Marks
				Theory	:	30 Marks
				Total	:	50 Marks
				Duration of Exam.	:	3 Hrs.

LIST OF EXPERIMENTS:

1. Design a CMOS Current Mirror in schematic and simulate for Transient Characteristics.
2. Design a CMOS Cascaded Current Mirror in schematic and simulate for Transient Characteristics.
3. Design a CMOS Common Source Amplifier with resistive load in schematic and simulate for Transient Characteristics.
4. Design a CMOS Common Source Amplifier with diode connected load in schematic and simulate for Transient Characteristics.
5. Design a CMOS Common Source Amplifier with current source load in schematic and simulate for Transient Characteristics.
6. Design a CMOS Common Drain Amplifier in schematic and simulate for Transient Characteristics.
7. Design a CMOS Common Gate Amplifier in schematic and simulate for Transient Characteristics.
8. Design the layout of a CMOS Common Source Amplifier with current source load.
9. Design the layout of a CMOS Current Mirror.
10. Design the layout of a CMOS Cascaded Current Mirror.
11. Design the layout of a CMOS Common Gate.

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTVLSI 504 contents.

`

MTVLSI 560 **IC FABRICATION TECHNOLOGY**

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

Cleanroom technology: Clean room concept – Growth of single crystal Si, surface contamination, cleaning & etching.& wafer preparation. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc

Epitaxy: Vapors phase Epitaxy ,Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics.

UNIT II

Oxidation: Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO_2

Diffusion: Diffusion from a chemical source invapor form at high temperature, diffusion from doped oxide source and diffusion from an ion implanted layer.

UNIT III

Lithography: Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X ray sources & masks. Ion lithography.

Etching: Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide, Trench etching.

Metallisation: Different types of metallisation, uses & desired properties

UNIT IV

Differential Metal gate transistor: Motivation, requirements, Integration Issues. Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, Single electron transistors, coulomb blockade effects in ultra-small metallic tunnel junctions .

Silicon on Insulator: Introduction of SOI, PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues, Vertical transistors**:** FinFET and Surround gate FET, 3D CMOS.

Text Books

1. S.M. Sze, "VLSI Technology", John Wiley & Sons, 2000.
2. S.M.Sze, Ed, High Speed Semiconductor Devices, Wiley, New York.

Reference Books:

1. S.M. Sze, Ed, Modern Semiconductor Device Physics, Wiley, New York
2. K. Seeger, Semiconductor Physics, 7th Ed, Springer-Verlag, Berlin,
3. C.Y. Chang and S.M. Sze, Eds, ULSI Devices, Wiley New York

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 570 **DSP FOR VLSI DESIGN**

L T P	Credits	Class Work	:	25 Marks
4 - -	4	Theory	:	75 Marks
		Total	:	100 Marks
		Duration of Exam.	:	3 Hrs.

UNIT I

VLSI for DSP: Data Flow graph representation, Iteration Bound, Pipelining and Parallelism; Re-timing techniques, Unfolding- algorithm, properties and applications of unfolding, Folding transformation, register minimization in folded architectures, folding of multirate systems

UNIT II

Architecture Design: DSP system architectures, Systolic Array Design Methodology, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit serial PEs. Pipelined and Parallel Architectures for Recursive and Adaptive Filters

UNIT III

Arithmetic Architectures: Bit level arithmetic architectures, redundant arithmetic, synchronous and asynchronous pipeline, low power design

UNIT IV

Case Study-TMS320CXX PROCESSOR: Architecture: Data formats, Addressing modes, Instruction sets and operations, Block diagram of DSP starter kit, Programs for processing real time systems

Text Books

1. K. K. Parhi, VLSI Digital Signal Processing Systems : Design and Implementation, Wiley,1999
2. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" -Tata McGraw Hill Publishing Company Limited. New Delhi, 2008

Reference Books:

1. P. Lapsley, J. Bier, A. Shoham and E. A. Lee, DSP Processor Fundamentals: Architectures and Features, Wiley/IEEE, 2001.
2. P. Pirsch, Architectures for Digital Signal Processing, Wiley, 1998.
3. T. Glokler and H. Meyr, Design of Energy-Efficient Application Specific Instruction Set Processors, Kluwer, 2004.
4. V. K. Madisetti, VLSI Digital Signal Processors, Butterworth-Heinemann/IEEE Press, 1995.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 580 INTRODUCTION TO MEMS

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

Historical Background: Silicon Pressure sensors, Micromachining, MicroElectroMechanicalSystems.; **Microfabrication and Micromachining**: Integrated Circuit Processes, Bulk Micromachining: Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA).

UNIT II

Physical Microsensors: Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples: Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors.
Microactuators: Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors-Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector.

UNIT III

Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials
Surface Micromachined Systems: Success Stories, Micromotors, Gear trains, Mechanisms.

UNIT IV

Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.;Lab/Design:(two groups will work on one of the following design project as a part of the course).;RF/Electronics device/system, Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays.

Text Books:

1. Stephen D. Senturia, "Microsystem Design" by, Kluwer Academic Publishers, 2001.

Reference Books:

1. Fundamentals of Microfabrication by, CRC Press, 1997.Gregory Kovacs, Micromachined Transducers Sourcebook WCB McGraw-Hill, Boston, 1998.
2. M.-H. Bao, Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes by Elsevier, New York, 2000.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 590 COMPUTATIONAL INTELLIGENT TECHNIQUES FOR VLSI DESIGN

L T P	Credits	Class Work	:	25 Marks
4 - -	4	Theory	:	75 Marks
		Total	:	100 Marks
		Duration of Exam.	:	3 Hrs.

UNIT I

Functions of a complex variable: Limit continuity and differentiability. Analytical functions, Cauchy-Riemann equations, Cauchy integral theorem, singularities Taylor's and Laurent Series, Conformal mapping.
Roots Finding for Non Linear equation: Functions and Polynomials, Zeros of a function, Roots of a nonlinear equation, Bracketing, Bisection and Newton-Raphson Methods, Polynomial fits.

UNIT II

Interpolation: Newton's (Newton-Gregory) Forwarded Difference (FD) Formula and Backward Difference (BD) Formula, Lagrange's divided differences and Newton's Divided Formula.
Numerical Integration: Evaluation of Integrals, Elementary Analytical Methods, Trapezoidal and Simpson's Rules, Gaussian Quadrature, and orthogonal polynomials, Multidimensional Integrals, Numerical differentiation and Estimation of errors.

UNIT III

Numerical Solution of Linear equation: Vectors and Matrices, Solutions of linear algebraic equations by direct and iterative methods, Gaussian elimination, LU, Cholesky and singular value decompositions, Matrix diagonalization methods.

UNIT IV

Numerical Methods for ordinary differential equation: Solution of initial-value problems of systems of ODEs, Single step and multistep methods, convergence. Finite difference methods for the solution of two-point boundary-value problem.

Text Books:

1. Murray R Spiegel, "Theory and Problems of Complex Variables", Schaum's Outline Series, New York, 1964.
2. Conte, S. D. de Boore, C. "Elementary Numerical Analysis" McGraw Hill, 1980.

References Books:

1. PradipNiyogi, "Numerical Analysis & Algorithms", TMH, 2003
2. Kreyszig, E, "Advanced Engineering Mathematics", John Wiley & Sons, 8th Edition, 2002
3. Radhey S Gupta, "Elements of Numerical Analysis", Macmillan, 2009.
4. Brian Bradie, "A Friendly Introduction to Numerical Analysis" Pearson, 2008
5. Chapra, S. C, Canale R P, "Numerical Methods for Engineers", 3rd Ed., McGraw-Hill 1998

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 601 CMOS MIXED SIGNAL CIRCUIT DESIGN

L	T	P	Credits			
4	-	-	4	Class Work	:	25 Marks
				Theory	:	75 Marks
				Total	:	100 Marks
				Duration of Exam.	:	3 Hrs.

UNIT I

PLL: Characterization of a comparator, basic CMOS comparator design, analog multiplier design, PLL - simple PLL, charge-pump PLL, applications of PLL,
Switched Capacitor Circuits: Switched Capacitor circuits - basic principles, some practical circuits such as switched capacitor integrator, biquad circuit, switched capacitor filter, switched capacitor amplifier, non-filtering applications of switched capacitor circuit such as programmable gate arrays, DAC and ADC, MOS comparators, modulators, rectifiers, detectors, oscillators.

UNIT II

Sampling Circuits: Sampling circuits: Basic sampling circuits for analog signal sampling, performance metrics of sampling circuits, different types of sampling switches. Sample-and-Hold Architectures: Open-loop & closed-loop architectures, open-loop architecture with miller capacitance, multiplexed-input architectures, recycling architecture, switched capacitor architecture, current-mode architecture.
DAC: Input/output characteristics of an ideal D/A converter, performance metrics of D/A converter, D/A converter in terms of voltage, current, and charge division or multiplication, switching functions to generate an analog output corresponding to a digital input. D/A converter architectures: Resistor-Ladder architectures, current-steering architectures.

UNIT III

ADC: Input/output characteristics and quantization error of an A/D converter, performance metrics of A/D converter. A/D converter architectures: Flash architectures, two-step architectures, interpolate and folding architectures, pipelined architectures, Successive approximation architectures, interleaved architectures.
Filters: Low Pass filters, active RC integrators, MOSFET-C integrators, transconductance-C integrator, discrete time integrators. Filtering topologies - bilinear transfer function and biquadratic transfer function.

UNIT IV

Data Converter SNR: Quantization Noise, Signal to Noise Ratio, improving SNR by using Averaging and Feedback.
Mixed-Signal Layout Issues: Floor planning, Power Supply and Ground Issues, Fully Differential Design, Guard Rings, Shielding, Other Interconnect Considerations

Text Books:

1. Razavi, "Design of analog CMOS integrated circuits", McGraw Hill, 2001
2. Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000

Reference Books

1. Jacob Baker, "CMOS Mixed-Signal circuit design", IEEE Press, 2002
2. Gregorian, Temes, "Analog MOS Integrated Circuit for signal processing", John Wiley & Sons
3. Baker, Li, Boyce, "CMOS : Circuit Design, layout and Simulation", PHI, 2000

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 657 MIXED SIGNAL IC DESIGN LAB

L	T	P	Credits		Class Work	:	20 Marks
-	-	3	1.5		Theory	:	30 Marks
					Total	:	50 Marks
					Duration of Exam.	:	3 Hrs

LIST OF EXPERIMENTS:

1. Design a Switched Capacitor Amplifier in schematic and simulate for Transient Characteristics.
2. Design a Switched Capacitor Low Pass Filter in schematic and simulate for Transient Characteristics.
3. Design Switched Capacitor High Pass Filter with resistive load in schematic and simulate for Transient Characteristics.
4. Design a Sample and Hold Circuits with diode connected load in schematic and simulate for Transient Characteristics.
5. Design RC integrators with current source load in schematic and simulate for Transient Characteristics.
6. Design MOS comparators in schematic and simulate for Transient Characteristics.
7. Design Sampling Switch in schematic and simulate for Transient Characteristics.
8. Design the layout of a Sampling Switch with current source load.
9. Design the layout of a Sample and Hold Circuits.
10. Design the layout of MOS comparators.
11. Design the layout of a Switched Capacitor Amplifier.

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTVLSI 601 contents.

`

MTVLSI 661 CMOS RF IC DESIGN

L T P	Credits			
4 - -	4	Class Work	:	25 Marks
		Theory	:	75 Marks
		Total	:	100 Marks
		Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

Modulation and Detection: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection**.**

UNIT II

RF transceivers: Receiver Architectures: Heterodyne Receiver, homodyne Receiver, Image-reject Receiver, Digital-IF Receiver, Sub sampling Receiver, RF Transmitters: Transmitter Architecture: direct-conversion Transmitters, Two-step Transmitters

RF Transistors: BJT and MOSFET Behavior at RF Frequencies Modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies.

UNIT III

RF circuits Design: Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, various mixers- working and implementation**.**

RF Oscillators: Basic LC Oscillators topologies, VCO, phase noise: effect, Mechanisms, Noise power and trade off, Bipolar and CMOS LC Oscillator designs, Quadrature signal and single sideband generators.

UNIT IV

RF Synthesizers: General Considerations, Phase-locked Loops: basic concept, Types of PLLs, Noise in PLLs , Various RF Synthesizer Architectures and Frequency Dividers.

RF Power Amplifier: General Considerations, Classification of Power Amplifiers, high frequency Power Amplifiers, Liberalization techniques.

.

Text Books:

1. Behzad Razavi, “RF Microelectronics”, Pearson Education.
2. Reinhold Ludwig, Paul Bretchko,“RF Circuit Design: Theory & Applications ”.

Reference Books

1. Thomas.H. Lee, “The design of CMOS Radio-Frequency Integrated Circuits”, Cambridge University Press, 2nd Edition, 2004.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 671 VLSI SIGNAL PROCESSING

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

INTRODUCTION TO DSP SYSTEMS: Introduction to DSP Systems-Typical DSP algorithms; Iteration Bound–data flow graph representations, loop bound & iteration bound, Longest path Matrix algorithm

PROCESSING: Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II

RETIMING: Retiming - definitions and properties; Unfolding – algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

FAST CONVOLUTION: Fast convolution–Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving.

UNIT III

FILTER PROCESSING: Look**-** Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

BIT-LEVEL ARITHMETIC ARCHITECTURES: Scaling and round-off noise- scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement.

UNIT IV

SYNCHRONOUS & ASYNCHRONOUS PIPELINING: Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining-synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol;

PROGRAMMING DIGITAL SIGNAL PROCESSORS : Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

Text Books:

1. Keshab K.Parhi, "VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic Publishers, 1998.

Reference Book:

1. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
2. S.Y. Kung, H.J. W. House, T. Kailath, "VLSI & Modern Signal Processing", Prentice Hall, 1985.
3. Jose E. France, Yannis Tsividis, "Design of Analog & Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 681 **SYSTEM ON CHIP**

L T P	Credits		Class Work	:	25 Marks
4 - -	4		Theory	:	75 Marks
			Total	:	100 Marks
			Duration of Exam.	:	3 Hrs.

UNIT I

Logic Gates: Introduction.Combinational Logic Functions.Static Complementary Gates. Switch Logic. Alternative Gate Circuits.Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect.

Combinational Logic Networks: Introduction.Standard Cell-Based Layout.Simulation.Combinational Network Delay. Logic and Interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.

UNIT II

Sequential Machines.: Introduction.Latches and Flip-Flops.Sequential Systems and Clocking Disciplines.Sequential System Design.Power Optimization. Design Validation. Sequential Testing.

Subsystem Design: Introduction.Subsystem Design Principles, Combinational Shifters, Adders, ALUs, Multipliers.High-Density Memory.Field-Programmable Gate Arrays, Programmable Logic Arrays.References.Problems.

UNIT III

Floor-planning: Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, Switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, The I/O Architecture, PAD Design.

UNIT IV

NOC DESIGN : Practical Design of NoC, NoC Topology-Analysis Methodology, Energy Exploration, NoC Protocol Design, Low-Power Design for NoC: Low-Power Signaling, On-Chip Serialization, Low-Power Clocking, Low-Power Channel Coding, Low-Power Switch, Low-Power Network on Chip Protocol

NOC /SOC CASE STUDIES : Real Chip Implementation-BONE Series-,BONE 1-4, Industrial Implementations-, Intel's Tera-FLOP 80-Core NoC, Intel's Scalable Communication Architecture, Academic Implementations-FAUST, RAW; design case study of SoC –digital camera

Text Book:

1. Wayne Wolf,“ Modern VLSI Design–System–on –Chip Design”, Prentice Hall, 3rd Ed., 2008.
2. Hoi-jun yoo, Kangmin Lee, Jun Kyoung kim, “Low power NoC for high performance SoC desing”,CRC press, 2008.

Reference Book:

1. Wayne Wolf, “Modern VLSI Design– IP based Design”, Prentice Hall, 4th Ed., 2008.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 691 **CAD FOR VLSI**

L	T	P	Credits			
4	-	-	4	Class Work	:	25 Marks
				Theory	:	75 Marks
				Total	:	100 Marks
				Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Introduction to CAD tools-Evolution of Design Automation-Basic Transistor Fundamentals-CMOS realizations of basic gates.

VLSI Design Methodologies: Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II

Modeling: Modeling techniques, Types of CAD tools and Introduction to logic simulation Verilog: Syntax, Hierarchical modeling and Delay modeling, Verilog constructs, Memory modeling.

Synthesis: synthesis - Synthesizable and Non Synthesizable constructs, Logic Optimization, Resource Sharing, Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT III

Logic and layout synthesis: Technology mapping, ASIC design methodology, FPGA based system design and prototyping, layout synthesis: the physical design, timing analysis, graph algorithms and their application in IC design.

High level SYNTHESIS: High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

UNIT IV

Simulation: Gate-level modeling and simulation, Switch-level modeling and simulation,

System level design: brief mention of System C and System Verilog.

Text Books:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley-India, 1999
2. Giovanni De Micheli, Synthesis and Optimization of Digital Circuits, Tata McGraw Hill, 1994

Reference Books

1. D.D Gajski et al., High Level Synthesis: Introduction to Chip and System Design, Kluwer Academic Publishers, 1992
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, Kluwer Academic Publisher
3. M. Sarrafzadeh and C.K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 663 DESIGN OF SEMICONDUCTOR MEMORY

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

Introduction to Advanced Semiconductor Memories: Overview, Developments & Directions.
SRAM Technologies: Basic SRAM Architecture & Cell Structures, SRAM selection Considerations, High Performance SRAMs, Advanced SRAM Architectures.

UNIT II

Low Voltage SRAMS, SOI SRAMS, BiCMOS SRAM, CAM.Memory Peripheral Circuitry: The Address Decoder, Sense Amplifier, Voltage References, Drivers / Buffers, Timing & Control, Memory Reliability & Yield. Power Dissipation in Memories – Sources of Power Dissipation, Partitioning of the Memory, Addressing the active power dissipation, Data Retention Dissipation.

UNIT III

DRAM: Technology & Evolution & Trends, DRAM Timing Specifications, EDO DRAMs, EDRAM, Synchronous DRAM, Enhanced Synchronous DRAM, Cache DRAM.

UNIT IV

Non-Volatile Memeory: Introduction, Floating Gate cell Theory & Operations, Charge Transport Mechanisms, and Nonvolatile Memory Cell & Array Design, UV-EPROM cells & EEPROM Cells, Flash Memory Cells.
Flash Memory Architectures: NOR, NAND, DINOR & AND Architecture Flash Memories. Multilevel Nonvolatile Memories, Ferroelectric Memories.

Text Books:

1. Ashok K Mishra , "Advanced Semiconductor Memories", IEEE Press, Wiley & Sons, 2009.
2. Jan M .Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd edition Prentice Hall Publication, 2011

Reference Books:

1. S. Kang & Y. Leblebici "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003.
2. Betty Prince, "Semiconductor Memories: A Handbook of Design, Manufacture and Application", John Wiley & Sons Publication.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 673 HIGH SPEED VLSI INTERCONNECTS

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

PRELIMINARY CONCEPTS OF VLSI INTERCONNECTS: Interconnects for VLSI applications, copper interconnections, method of images, method of moments, even and odd capacitances, transmission line equations, miller's theorem, Resistive interconnects as ladder network, Propagation modes in micro strip interconnects, slow wave propagations, Propagation delay.

UNIT II

PARASITIC RESISTANCES, CAPACITANCE AND INDUCTANCES: Parasitic resistances, capacitances and inductances, approximate formulas for inductances, green's function method, using method of images and Fourier integral approach, network Analog method, Inductance extraction using fast Henry, copper interconnections for resistance modelling .

UNIT III

INTERCONNECTION DELAYS : Metal insulator semiconductor micro strip line, transmission line analysis for single level interconnections, transmission line analysis for parallel multilevel interconnections, analysis of crossing interconnections, parallel interconnection models for micro strip line, modelling of lossy parallel and crossing interconnects, high frequency losses in micro strip line, Expressions for interconnection delays, Active interconnects.

UNIT IV

CROSS TALK ANALYSIS: Lumped capacitance approximation, coupled multi conductor MIS micro strip line model for single level interconnects, frequency domain level for single level interconnects, transmission line level analysis of parallel multi-level interconnections.

NOVEL SOLUTIONS FOR PROBLEMS IN INTER: Optical interconnects – carbon Nano tubes / Graphenes vs. Copper wires.

Text Books:

1. H B Bakog Lu, Circuits, "Interconnections and packaging for VLSI",Addison Wesley publishing company.
2. J A Davis, J D Meindl, "Interconnect technology and design for Gigascale integration", Kluwer academic publishers.

Reference Books:

1. Nurmi J, Tenhumen H, Isoaho J, Jantsch A, "Interconnect Centric deisgn for advanced SOC and NOC", Springer.
2. C K Cheng, J Lillis, S Lin, N Chang, "Interconnect analysis and synthesis", Wiley inter-science.
3. Hall S H, G W Hall and J McCall, High speed digital system design, Wiley inter-science
4. Askok K Goel, "High speed VLSI interconnections", Wiley Interscience, second edition, 2007

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 683 HARDWARE SOFTWARE CO-DESIGN

L T P	Credits			
4 - -	4	Class Work	:	25 Marks
		Theory	:	75 Marks
		Total	:	100 Marks
		Duration of Exam.	:	3 Hrs.

UNIT I

Introduction: Motivation hardware & software co-design, system design consideration, research scope & overviews. Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance modeling, Hardware Software development.

UNIT II

Hardware Software co-design research: An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment. Co-design concepts: Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software trade-offs, co-design.

UNIT III

Methodology for co-design: Amount of unification, general consideration & basic philosophies, a framework for co-design. Unified representation for Hardware & Software: Benefits of unified representation, modeling concepts. An abstract Hardware & Software model : Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model.

UNIT IV

Performance evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation. Object oriented techniques in hardware design: Motivation for object oriented technique, data types, modelling hardware components as classes, designing specialized components, data decomposition, Processor example.

Text Books:

1. Sanjaya Kumar, James H. Ayler "The Co-design of Embedded Systems: A Unified Hardware Software Representation", Kluwer Academic Publisher, 2002.
2. H. Kopetz, Real-time Systems, Kluwer, 1997.

Reference Books:

1. R. Gupta, Co-synthesis of Hardware and Software for Embedded Systems, Kluwer 1995.
2. S. Allworth, Introduction to Real-time Software Design, Springer-Verlag, 1984.
3. Peter Marwedel, G. Goosens, Code Generation for Embedded Processors, Kluwer Academic Publishers, 1995.

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 693 ALGORITHM FOR VLSI DESIGN

L	T	P	Credits		Class Work	:	25 Marks
4	-	-	4		Theory	:	75 Marks
					Total	:	100 Marks
					Duration of Exam.	:	3 Hrs.

UNIT I

Logic synthesis & verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.
Partitioning: problem formulation, cost function and constraints, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT II

Floor planning & pin assignment: Floor planning model and cost function, Classification of Floor planning, constraint based floor planning, Integer Programming Based Floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.
Placement: problem formulation, cost function and constraints, simulation base placement algorithms, Partitioning Based Placement Algorithms, other placement algorithms,
.

UNIT III

Global Routing: Grid Routing and Global routing, Problem formulation, cost function and constraints, classification of global routing algorithms, routing regions, sequential global routing, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, Integer Programming Based Approach, Hierarchical Global Routing, Global Routing by Simulated Annealing
Detailed routing: problem formulation, cost function and constraints, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

UNIT IV

Over the cell routing & via minimization: Over-the-cell Routing: Cell Models, two layers over the cell routers, Three-Layer Over-the-cell Routing, constrained & unconstrained via minimization.
Compaction: problem formulation, Classification of Compaction Algorithms one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text Books:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.

Reference Books:

1. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition.
2. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

NOTE:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

`

MTVLSI 653 SEMINAR

L	T	P	Credits		Class Work	:	50 Marks
-	-	2	2		Exams	:	--
					Total	:	50 Marks

The objectives of the course remain:

- To learn how to carry out literature search
- To learn the art of technical report writing
- To learn the art of verbal communication with the help of modern presentation techniques

A student will select a topic in emerging areas of Engineering & Technology and will carry out the task under the supervision of a teacher assigned by the department.

He/ She will give a seminar talk on the same before a committee constituted by the chairperson the department. The committee should comprise of 2 or 3 faculty members from different specializations. The teacher(s) associated in the committee will each be assigned 2 hours teaching load per week.

However, supervision of seminar topic will be in addition to the regular teaching load.

`

MTVLSI 651 **DISSERTATION (PHASE-I)**

L	T	P	Credits	Class Work	:	100 Marks
-	-	6	6	Exams	:	--
				Total	:	100 Marks

The primary objective of this course is to develop in student the capacity for analysis & judgment and the ability to carry out independent investigation in design /development through a dissertation work involving creativity, innovation and ingenuity. The work must start with comprehensive literature search and critical appreciation thereof so as to select research problem the student wishes to work on.

Each student will carry out independent dissertation under the supervision of some teacher(s) who will be called Supervisor(s). In no case more than two supervisors can be associated with one dissertation work.
The dissertation involving design/ fabrication/ testing/ computer simulation/ case studies etc. which commences in the III Semester will be completed in IV Semester. The evaluation of the dissertation phase–I besides approval of the dissertation topic of the students will be done by a committee constituted as under:

Chairperson of Department	: Chairperson
M Tech Coordinator/ Sr Faculty	: Member Secretary
Respective dissertation supervisor	: Member

The student will be required to submit two copies of his/her report to the department for record (one copy each for the department and participating teacher).

.

`

MTVLSI 652 DISSERTATION

L	T	P	Credits		Class Work	:	50 Marks
-	-	20	20		Exams	:	100 Marks
					Total	:	150 Marks

The dissertation started in III Semester will be completed in IV Semester and will be evaluated in the following manner.

Internal Assessment

Internal Assessment (class work evaluation) will be effected as per ordinance through interim report, presentation and discussion thereon by the following committee of three persons:

Chairperson of Department : Chairperson

M Tech Coordinator/ Sr Faculty : Member Secretary

Respective dissertation supervisor : Member

External Assessment

Final dissertation will be assessed by a panel of examiners consisting of the following:

Chairperson of Department : Chairperson

Respective Supervisor(s) : Member(s)

External expert : To be appointed by the University

NOTE: The External Expert must be from the respective area of specialization. The chairperson & M Tech Coordinator with mutual consultation will divide the submitted dissertations into groups depending upon the area of specialization and will recommend the list of experts for each group separately to the V C for selecting the examiners with the note that an external expert should be assigned a maximum of FIVE dissertations for evaluation.

The student will be required to submit THREE copies of his/her report to the M Tech Coordinator for record and processing.