Name of Faculty : **Rekha Yadav, ECED**

Discipline : **M.Tech. ECE (VLSI Design)**

Semester : **2nd Semester.**

Subject : **Analog CMOS IC Design**

Lesson Plan Duration : **15 Weeks (8th Jan. 2018 to 27th April 2018)**

Work Load per week : **Lecture-04, Practical:-01**

Course Objective:

1. To develop the ability design and analyze MOS based Analog VLSI circuits to draw the equivalent circuits of MOS based Analog VLSI and analyze their performance.
2. To develop the skills to design analog VLSI circuits for a given specification.
3. To deals with Basic theory of Analog Circuits, Design principles and techniques for analog IC's blocks implemented in CMOS technology
4. To learn about Device Modeling- Various types of analog systems- CMOS amplifiers and Comparator.

Week	Theory		Practical	
	Lecture Day	Topic	Practical Day	Topic
1st	1st	➢ MOS IV Characteristics	1st	➢ Basic about tool used
	2nd	➢ Second order effects,		
	3rd	➢ Short-Channel Effects,		
	4th	➢ MOS Device Models		
2nd	5th	➢ Review of Small Signal MOS Transistor Models	2nd	➢ Design a CMOS Current Mirror in schematic and simulate for Transient Characteristics
	6th	➢ MOSFET Noise.		
	7th	➢ **CMOS Sub circuits**,		
	8th	➢ MOS Switch		
3rd	9th	➢ MOS Diode	3rd	➢ Design a CMOS Cascaded Current Mirror in schematic and simulate for Transient Characteristics.
	10th	➢ MOS Active Resistors,		
	11th	➢ Current Sources		
	12th	➢ CMOS Regulated Cascade current source		
4th	13th	➢ Cascade current sink	4th	➢ Design a CMOS Common Source Amplifier with resistive load in schematic and simulate for Transient Characteristics.
	14th	➢ Basic of current mirror		
	15th	➢ Simple current mirror		
	16th	➢ Cascode current Mirror		
5th	17th	➢ Widlar current mirror	5th	➢ Design a CMOS Common Source Amplifier with diode connected load in schematic and simulate for Transient Characteristics.
	18th	➢ Wilson Current Mirror		
	19th	➢ Miller Effect,		
	20th	➢ Association of Poles with nodes,		
6th	Class test and minor test -1			
7th	21st	➢ Frequency Response of all single stage amplifiers.	6th	➢ Design the layout of a CMOS Common Source Amplifier with current source load.
	22nd	➢ Common Drain		
	23rd	➢ Common Gate		
	24th	➢ Common Source Amplifiers – resistive load		
8th	25th	➢ diode connected load, current source load,	7th	➢ Design the layout of a CMOS Current Mirror.

	26th	➢ triode load, source degeneration		
	27th	➢ Simple Inverting Amplifier, Gilbert Cell		
	28th	➢ Cascade Amplifier,		
9th	29th	➢ source follower.	8th	➢ Design the layout of a CMOS Cascaded Current Mirror.
	30th	➢ Differential Amplifiers,		
	31st	➢ Output Amplifiers,		
	32nd	➢ Applications of operational Amplifier,		
10th	33rd	➢ theory and Design;	9th	➢ Design the layout of a CMOS Common Gate.
	34th	➢ Definition of Performance Characteristics;		
	35th	➢ Design of two stage MOS Operational Amplifier		
	36th	➢ two stage MOS operational Amplifier with cascades.		
11th	37th	➢ MOS telescopic-cascode operational amplifiers,	10th	➢ Design a CMOS Common Source Amplifier with current source load in schematic and simulate for Transient Characteristics.
	38th	➢ MOS Folded-cascade operational amplifiers		
	39th	➢ gain boosting		
	40th	➢ Comparison of various topologies,		
12th	41st	➢ noise in op-amps	11th	➢ Design a CMOS Common Drain Amplifier in schematic and simulate for Transient Characteristics.
	42nd	➢ op-amp stability		
	43rd	➢ frequency compensation.		
	44th	➢ Comparators Models and Performance,		
13th	➢ Class test and Minor Test -2			
14th	45th	➢ Development of a CMOS Comparator,	12th	➢ Practice and performed all practical's
	46th	➢ Design of a Two-Stage CMOS Comparator.		
	47th	➢ Other Types of Comparators.		
	48th	➢ Voltage controlled oscillator		
15th	49th	➢ Sampling Switches,	13th	➢ Internal Practical viva
	50th	➢ Switched Capacitor Amplifier		
	51st	➢ Switched Capacitor integrator.		
	52nd	➢ Switched Capacitor filters.		

Course Outcome:

At the completion of this course, each student will have demonstrated proficiency in:

1. Designing CMOS analog circuits to achieve performance specifications;
2. Working as a team to design, implement, and document an analog integrated circuit.
3. Ability to analyze, design and evaluate microelectronic integrated circuits
4. Analysis of switched capacitor circuits and voltage controlled oscillator.

Text Books:

1. Behzad Razavi, " Design of Analog CMOS Integrated Circuit", Mc Graw-Hill
2. Allen and Holberg, "CMOS Analog Circuit Design"

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Reference Books:

1. D. A. Johns and Martin, "Analog Integrated Circuit Design", John Wiley, 1997.
2. Gregorian and G C Temes, "Analog MOS Integrated Circuits for Signal Processing", John Wiley, 1986.
3. R L Geiger, P E Allen and N R Strader, VLSI Design Techniques for Analog & Digital Circuits, McGraw Hill, 1990.

MTVLSI 503B IC FABRICATION TECHNOLOGY

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks
Duration of Exam.	:	3 Hrs.

Course Objective:
OBJECTIVES:

1. This course aims at understanding the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication.
2. To introduce the fundamentals of IC fabrication technology, IC chip size and circuit complexity etc.
3. Provide a strong foundation on Linear Circuits.
4. Familiarize students with applications of various IC's.

OUTCOME:

1. The students passing this course will be proficient in the concepts of fabrication of IC technology.
2. Build circuits using IC's.
3. In-depth knowledge of applying the concepts in real time applications.
4. Understand the main elements of hierarchical IC design namely interested circuit technology, approaches to system design, architectural issues, design implementation and layout.

Books :

1. S.M. Sze, "VLSI Technology", John Wiley & Sons, 2000.
2. S.M.Sze, Ed, High Speed Semiconductor Devices, Wiley, New York.
3. S.M. Sze, Ed, Modern Semiconductor Device Physics, Wiley, New York
4. K. Seeger, Semiconductor Physics, 7th Ed, Springer-Verlag, Berlin,
5. C.Y. Chang and S.M. Sze, Eds, ULSI Devices, Wiley New York

LECTUREWISE PROGRAMME : (from 08.01.18 to 27.04.18)

Introduction of the subject (08.01.18)	1
UNIT- I	
CLEANROOM TECHNOLOGY (09.01.18 to 20.01.18)	
Clean room concept – Growth of single crystal Si,	1
surface contamination, cleaning & etching.& wafer preparation	1
Processing considerations: Chemical cleaning	1
Modeling thermal Stress factors	2
EPITAXY (23.01.18 to 31.01.18)	
Vapors phase Epitaxy ,Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers,	2
epitaxial defects, molecular beam epitaxy, equipment used, film characteristics.	2
UNIT- II	
OXIDATION and DIFFUSION (02.02.18 to 23.02.18)	
Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides.	4
Oxidation technique & systems dry & wet oxidation. Masking properties of SiO2	2
Diffusion from a chemical source in vapor form at high temperature,	2
Diffusion from doped oxide source and diffusion from an ion implanted layer.	2
UNIT – III	
LITHOGRAPHY and METALLISATION (26.02.18 to 14.03.18)	
Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation	2
Electron optics: roster scans & vector scans, variable beam shape.	2
X-ray lithography: resists & printing, X ray sources & masks. Ion lithography	2
Different types of metallisation, uses & desired properties	1
ETCHING (16.03.18 to 26.03.18)	
Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching	2
Ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes:	2

poly/polycide, Trench etching.

UNIT – IV

DIFFERENTIAL METAL GATE TRANSISTOR (27.03.18 to 17.04.18)

Motivation, requirements, Integration Issues.	1
Transport in Nano MOSFET, velocity saturation, ballistic transport.	2
Injection velocity, velocity overshoot.	2
Single electron transistors.	1
Coulomb blockade effects in ultra-small metallic tunnel junctions.	1

SILICON ON INSULATOR (18.04.18 to 27.04.18)

Introduction of SOI, PDSOI and FDSOI,	1
Ultrathin body SOI - double gate transistors	1
Integration issues, Vertical transistors**:** FinFET, Surround gate FET, 3D CMOS	1

Home Assignments : 4 –5 assignments are given during the semester.

Evaluation Procedure

1.	Surprise Quiz/ Tutorial Test	5 Marks
2.	Assignment / Project / Performance in the Class	5 Marks
3.	Minor Tests (Two tests having equal weightage) Minor Test I : 14-16 Feb, 2018 Minor Test II : 4 -6 April, 2018	15 Marks
4.	Major test (University Examination)	75 Marks

Award of Grades Based on Absolute Marks: The University is following the system of grading based on absolute marks (after applying moderation if any). Following grading will be done based on the % of marks obtained in all the components of evaluation part of the subject. A+ (90% - 100 %), A (80% - 89%), B+ (70% - 79%) , B(62% - 69%), C+ (55% - 61%),C (46% - 54%), D (40% - 45), F (Less than 40 %)

For F grade, a candidate shallbe required to appear in the major test of concerned course only in the subsequent examination(s) to obtain the requisite marks/grade.

Attendance Record – Candidate should attend at least75% attendance of the total classes held of the subject

Chamber consultation hour: Any vacant period.

Note:

In the semester examination, the examiner will select two questions from each unit (total eight questions in all), covering the entire syllabus. The student will be required to attempt five questions, selecting at least one question from each unit.

(Ms. Himanshi Saini)

LOW POWER VLSI DESIGN (MTVLSI 508)

L	T	P	Class Work	:	25 marks	Duration of Exam	:
	3 hrs						
4	0	0	Exam	:	75 marks	Credits	
	:	4					
			Total	:	100 marks		

Objective & Scope of the course: This course is intended to keep the student abreast of the followings:

1. Need for low power VLSI chips and Device & Technology Impact on Low Power
2. Simulation Techniques for Power analysis
3. Low Power Techniques, Architecture & Systems

Lecture Plan

Lecture 1	Introduction to Low Power VLSI Design
Lecture 2	Need for low power VLSI chips
Lecture 3	Sources of power dissipation on Digital Integrated circuits
Lecture 4	Emerging Low power approaches
Lecture 5	Physics of power dissipation in CMOS devices
Lecture 6	Device & Technology Impact on Low Power
Lecture 7	Dynamic dissipation in CMOS
Lecture 8	Transistor sizing & gate oxide thickness,
Lecture 9	Impact of technology Scaling, Technology & Device innovation
Lecture 10	Power estimation Techniques
Lecture 11	Introduction to simulation Power analysis
Lecture 12	SPICE circuit simulators
Lecture 13	gate level logic simulation
Lecture 14	capacitive power estimation
Lecture 15	static state power
Lecture 16	gate level capacitance estimation
Lecture 17	architecture level analysis
Lecture 18	data correlation analysis in DSP systems
Lecture	Monte Carlo simulation

19	
Lecture 20	Probabilistic power analysis: Random logic signals
Lecture 21	Probabilistic power analysis: probability & frequency
Lecture 22	Probabilistic power analysis: probabilistic power analysis techniques, signal entropy
Lecture 23	Probabilistic power analysis: signal entropy
Lecture 24	Introduction to Low Power Techniques
Lecture 25	Circuit level: Power consumption in circuits
Lecture 26	Circuit level: Flip Flops & Latches design
Lecture 27	Circuit level: high capacitance nodes
Lecture 28	Circuit level: low power digital cells library
Lecture 29	Logic level: Gate reorganization
Lecture 30	Logic level: signal gating
Lecture 31	Logic level: logic encoding
Lecture 32	Logic level: state machine encoding
Lecture 33	Logic level: pre-computation logic
Lecture 34	Introduction to Low power Architecture & Systems
Lecture 35	Power & performance management
Lecture 36	switching activity reduction
Lecture 37	parallel architecture with voltage reduction
Lecture 38	flow graph transformation
Lecture 39	low power arithmetic components
Lecture 40	low power memory design
Lecture 41	Introduction to Low power Clock Distribution
Lecture 42	Power dissipation in clock distribution
Lecture	single driver Vs distributed buffers

43	
Lecture 44	Zero skew Vs tolerable skew
Lecture 45	Chip & package co design of clock network.

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Outcomes: The students are acquainted with the knowledge of the followings:

1. Low power VLSI chips, Device & Technology and Simulation Techniques for Power analysis
2. Low Power Techniques, Architecture & Systems

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MTVLSI504 ESD USING AVR MICROCONTROLLER

L	T	P	Credits		
4	-	-	04	Sessional Marks: 25	
				Theory Marks:	75
				Duration of Exams:	3 Hours

OBJECTIVES:

1. To Review the Basic Concept of Embedded Systems**.**
2. To Develop an Intuitive Understanding of Microcontrollers and Microprocessors.
3. To Study the Software for Embedded System Design
4. To Analyze the Architecture of Microcontrollers and to Understand the AVR Microcontrollers.
5. To Study Various Features of AVR Microcontrollers.
6. To Get the Idea of Assembly Language Programming/C for Microcontrollers.
7. To Develop and Understand Various Applications Using Microcontrollers

OUTCOME:

5. Able to Know the Basic Concept of Embedded Systems**.**
6. Able to Know the difference between Microcontrollers and Microprocessors.
7. Able to Know the Software for Embedded System Design
8. Able to Know the Architecture of AVR Microcontrollers.
9. Able to Know Various Features of AVR Microcontrollers.
10. Able to do Assembly Language Programming/C for Microcontrollers.
11. Able to Develop and Understand Various Applications Using Microcontrollers

Books :

Text Books:

1. Dananjay V. Gadre, Programming and Customizing the AVR microcontroller", McGraw Hill 2001.

Reference Books:

1. John.B..Peatman, "Design with PIC Micro controller", Pearson Education, 1988.
2. Embedded C Programming and the Atmel AVR; Richard H Barnett, Sarah Cox, Larry O'Cull; 2006
3. C Programming for Microcontrollers Featuring ATMEL's AVR Butterfly and WinAVR Compiler; Joe Pardue; 2005.
4. Atmel AVR Microcontroller Primer*:* Programming & Interfacing; Steven F Barrett, Daniel Pack, Mitchell Thornton; 2007.

LECTUREWISE PROGRAMME : (from 08.01.18 to 27.04.18)

Introduction of the subject (08.01.18)	1
UNIT- I	
INTRODUCTION OF EMBEDDED SYSTEMS(09.01.18 to 20.01.18)	
Definition, ingredients of embedded system	1
Requirements & challenges of embedded system design	1
Different types of microcontrollers: Embedded microcontrollers	2
External memory microcontrollers etc., processor architectures: Harvard V/S Princeton, CISC V/S RISC	3
The Cellular Concept-System Design Fundamentals (23.01.18 to 31.01.18)	
Microcontroller's memory types	3
Microcontrollers features: clocking, i/o pins, Pin Diagram	2
interrupts, timers, and peripherals	2
UNIT- II	
SOFTWARE FOR EMBEDDED SYSTEM DESIGN(02.02.18 to 23.02.18)	
Development tools/environments, Assembly language programming style, Interpreters, High level languages, Intel hex format object files, Debugging	3+3
Basic Programme Practicei.e Addition, Subtraction etc.	2
Complex Programmes Practice	3

UNIT – III

AVR MICROCONTROLLER(26.02.18 to 14.03.18)

Introduction to AVR microcontroller, features of AVR family microcontrollers,	2
Different types of AVR microcontroller	2
Architecture, memory access and instruction execution	2
Pipelining, program memory considerations, addressing modes, CPU registers, Instruction set, and simple operations	3

FEATURES OF AVR MICROCONTROLLER(16.03.18 to 26.03.18)

Timer: Control Word, mode of timers, simple programming,	2
Generation of square wave, Interrupts**:**Introduction, Control word Simple Programming, generation of waveforms using interrupt	2
Serial interface using interrupt, Watch-dog timer,Power-down modes of AVR microcontroller, UART, SRAM.	2

UNIT – IV

APPLICATION BASED AVR MICROCONTROLLER(27.03.18 to27.04.18)

Interfacing of AVR microcontroller with other devices using serial / parallel communication	2
I2C Protocol	1
SPI Protocol	1
ADC/DAC	2
DC motor controller using PWM	2
Practice to Programming	4

Home Assignments : 3-4 assignments are given during the semester.

Evaluation Procedure

1.	Surprise Quiz/ Tutorial Test	5 Marks
2.	Assignment / Project / Performance in the Class	5 Marks
3.	Minor Tests (Two tests having equal weightage) Minor Test I :14-16 Feb, 2018 Minor Test II :4 -6 April, 2018	15 Marks
4.	Major test (University Examination)	75 Marks

Award of Grades Based on Absolute Marks: The University is following the system of grading based on absolute marks (after applying moderation if any). Following grading will be done based on the % of marks obtained in all the components of evaluation part of the subject.

A+ (90% - 100 %), A(80% - 89%), B+ (70% - 79%) , B(62% - 69%), C+ (55% - 61%),C (46% - 54%), D (40% - 45), F (Less than 40 %)

For F grade, a candidate shallbe required to appear in the major test of concerned course only in the subsequent examination(s) to obtain the requisite marks/grade.

Attendance Record – Candidate should attend at least75% attendance of the total classes held of the subject

Chamber consultation hour: Any vacant period.

Note:

1. In the semester examination, the examiner will set 08 questions in all selecting two from each unit (1 & 2 from unit I, 3 & 4 from unit II, 5 &6 from unit III and 7 & 8 from unit IV). The students will be required to attempt only 5 questions selecting at least one question from each unit. All questions will carry equal marks.
2. The use of scientific calculator will be allowed in the examination. However, programmable calculator and cellular phone will not be allowed.
3. The use of properties (water, air, steam etc) tables, heat transfer tables, charts is permitted

(Dr. RajeshwarDass)

MTVLSI504 ESD USING AVR MICROCONTROLLER

L	T	P	Credits
-	-	3	1.5

Class Work	:	20 Marks
Theory	:	30 Marks
Total	:	50 Marks
Duration of Exam.	:	3 Hrs.

OBJECTIVES:

1. To Review the Basic Concept of Embedded Systems**.**
2. To Develop an Intuitive Understanding of Programming of Microcontrollers
3. To Study the Software for Embedded System Design
4. To Get the Idea of Assembly Language Programming**/**C for Microcontrollers**.**
5. To Develop and Understand Various Applications Using Microcontrollers

OUTCOME:

1. Able to Know the Basic Concept of Embedded Systems**.**
2. Able to Know the difference between Microcontrollers and Microprocessors**.**
3. Able to Know the Software for Embedded System Design
4. Able to do Assembly Language Programming**/**C for Microcontrollers**.**
5. Able to Develop and Understand Various Applications Using Microcontrollers

Books :

1. Dananjay V. Gadre, Programming and Customizing the AVR microcontroller," McGraw Hill 2001.
2. John.B..Peatman, "Design with PIC Micro controller", Pearson Education, 1988.
3. Embedded C Programming and the Atmel AVR; Richard H Barnett, Sarah Cox, Larry O'Cull; 2006
4. C Programming for Microcontrollers Featuring ATMEL's AVR Butterfly and WinAVR Compiler; Joe Pardue; 2005.
5. Atmel AVR Microcontroller Primer: Programming & Interfacing; Steven F Barrett, Daniel Pack, Mitchell Thornton; 2007.

LABPROGRAMME : (from 10.01.18 to 26.04.18)

Introduction of the Lab (10.01.18) 1

Experiments

ESD USING AVR MICROCONTROLLER LAB(10.01.18 to 26.01.18)

1. To study the architecture of AVR Microcontroller & AVR development board. 1
2. Write an ALP to enter a word from keyboard and to display. 1
3. Write an ALP to generate 10 KHz& 100KHz frequency using AVR Microcontroller. 2
4. Write an ALP to interface intelligent LCD display. 1
5. Write an ALP to interface intelligent LED display. 1
6. Write an ALP to Switch ON alarm when AVR Microcontroller receive interrupt. 1
7. Write an ALP to interface AVR microcontroller with other using serial / parallel communication. 1
8. Write an ALP to I2C Protocol interface. 1
9. Write an ALP to interface ADC/DAC. 1
10. Write an ALP to interface DC motor controller using PWM. 1

Home Assignments : 3-4 assignments are given during the semester.

Evaluation Procedure

1.	Surprise Quiz/ Tutorial Test	5 Marks

2.	Assignment / Project / Performance in the Class	5 Marks
3.	File	5 Marks
4	Internal Viva	5 Marks
5	Theory Test	30 Marks

Award of Grades Based on Absolute Marks: The University is following the system of grading based on absolute marks (after applying moderation if any). Following grading will be done based on the % of marks obtained in all the components of evaluation part of the subject.
A+ (90% - 100 %), A(80% - 89%), B+ (70% - 79%) , B(62% - 69%), C+ (55% - 61%),C (46% - 54%), D (40% - 45), F (Less than 40 %)

For F grade, a candidate shallbe required to appear in the major test of concerned course only in the subsequent examination(s) to obtain the requisite marks/grade.

Attendance Record – Candidate should attend at least75% attendance of the total classes held of the subject
Chamber consultation hour: Any vacant period.

NOTE:

7 experiments are to be performed from the above list. Remaining 3 can be performed depending upon the infrastructure available and MTVLSI 504 contents.

(Dr. RajeshwarDass)